PATENT ABSTRACTS OF JAPAN

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(71)Applicant : SEIKOSHA CO LTD

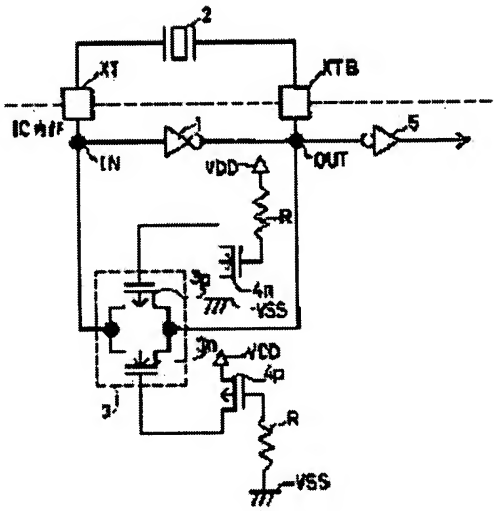
(72)Inventor : NAKAMURA HIDEYUKI

(54) OSCILLATION USE INTEGRATED CIRCUIT AND OSCILLATION CIRCUIT

(57)Abstract:

PURPOSE: To obtain an oscillation use integrated circuit and an oscillation circuit with excellent durability against static electricity without increasing the circuit area.

CONSTITUTION: A crystal resonator 2 is mounted externally between an input terminal and an output terminal of a CMOS inverter 1, and a feedback resistor comprising MOS transistors(TRs) 3n, 3p is connected between the input terminal and an output terminal of the CMOS inverter 1. Since gates of the MOS Trs 3n, 3p are kept to a desired potential via MOS Trs 4p, 4n respectively, when a static electricity intrudes from external terminals XT, XTB used for the connection of the crystal vibrator 2, an overvoltage applied to the gates of the MOS Trs 3n, 3p is reduced via MOS Trs 4p, 4n to avoid destruction of the gates.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the integrated circuit for an oscillation, and an oscillator circuit.
[0002]
[Description of the Prior Art] Now, in the integrated circuit for an oscillation used as a reference clock generation source by the clock etc., piezoelectric transducers, such as a quartz resonator, are connected between the input/output terminals of a CMOS inverter, and the feedback resister is further connected between the input/output terminals of a CMOS inverter. There is a thing as there are some which constituted the feedback resister from an MOS transistor among such things, for example, shown in drawing 2. This has connected between the input/output terminals of CMOS inverter 22 by which external was carried out in the quartz resonator 21 between the input terminal in and the output terminal out through P channel type MOS transistor23p and 23n of N channel type MOS transistors. Through Resistance r, it has connected with the power terminal VDD (for example, +5v) and the power terminal VSS (for example, 0v), respectively, and these operate the gate of these MOS transistors 23n and 23p as a feedback resister by the on resistance. In addition, in this drawing, 24 is an output buffer and sends an oscillation output signal to the latter part (not shown) in response to the output of CMOS inverter 22. Moreover, xt and xtb are the external terminals for carrying out external [of the quartz resonator 21].
[0003]
[Problem(s) to be Solved by the Invention] In such a thing, the gate of MOS transistors 23n and 23p is connected to a power terminal through Resistance r. Since the chip size of such an integrated circuit for an oscillation is made to increase, the resistance of this resistance r can seldom be enlarged. Moreover, since it is carrying out external [of the quartz resonator 21] to CMOS inverter 22, the close terminal in and output terminal out of CMOS inverter 22 are exposed to external static electricity. for this reason, with external static electricity, when the overvoltage joined the input terminal in or the output terminal out, it was alike occasionally that the gate of MOS transistors 23n or 23p is destroyed, and it was done
[0004] Then, the purpose of this invention is to offer the integrated circuit for an oscillation and an oscillator circuit excellent in the endurance over static electricity, without making circuit area increase.
[0005]
[Means for Solving the Problem] A CMOS inverter is provided, and in the integrated circuit for an oscillation by which external is carried out in a piezoelectric transducer between the input/output terminals of the above-mentioned CMOS inverter, while connecting the feedback resister which consists of an MOS transistor between the input/output terminals of the above-mentioned CMOS inverter, the gate of the above-mentioned MOS transistor is held to specific potential through the 2nd MOS transistor.
[0006] While connecting the feedback resister which consists of an MOS transistor between the input/output terminals of the above-mentioned CMOS inverter in the oscillator circuit which comes to connect a piezoelectric transducer between the input/output terminals of the above-mentioned CMOS inverter while connecting load-carrying capacity to each of the input terminal of a CMOS inverter and the above-mentioned CMOS inverter, and an output terminal, the gate of the above-mentioned MOS transistor is held to specific potential through the 2nd MOS transistor.
[0007] The above attains the above-mentioned purpose.
[0008]
[Example] Next, one example of this invention is explained. Drawing 1 is the electrical diagram showing the composition of this example, in this drawing, 1 is a CMOS inverter and external [of the quartz resonator 2 as a piezoelectric transducer] is carried out through the external terminals XT and XTB between the input terminal IN of this CMOS inverter 1, and an output terminal OUT. Moreover, although not illustrated, the capacitor as load-carrying

capacity is connected to an input terminal IN and an output terminal OUT. 3n and 3p are N channel type and P channel type MOS transistors, respectively. Between the input terminal IN of CMOS inverter 1 and an output terminal OUT is connected through MOS transistors 3n and 3p, and these MOS transistors 3n and 3p constitute a feedback resister 3. 4n and 4p are N channel type and P channel type MOS transistors, respectively, and these are the 2nd MOS transistor. The drain of MOS transistors 4n and 4p is connected to the MOS transistors [3p and 3n] gate, respectively, the source of these MOS transistors 4n and 4p is connected to power terminals VSS (0v) and VDD (5v), respectively, and the gate is connected to power terminals VDD and VSS through Resistance R, respectively. By setting up suitably transistor sizes, such as voltage impressed to the gate of these MOS transistors 4n and 4p or gate length, and gate width, the on resistance of MOS transistors 4n and 4p can be set as a desired value, and is set as the big value here compared with the resistance (for example, it consists of diffused resistors etc.) connected to the gate of the MOS transistor which accomplishes the feedback resister in the conventional integrated circuit for an oscillation. In addition, 5 is an output buffer and sends an oscillation output signal to the latter part (not shown) in response to the output of CMOS inverter 1. Here, although [the above composition] it integrates to the same IC substrate except for a quartz resonator 2, not only this but the output buffer 5 may be formed outside, or it may carry out external [of the above-mentioned capacitor].

[0009] Next, operation of this example constituted as mentioned above is described.

[0010] First, if the gate of MOS transistors 4n and 4p is connected to power terminals VDD and VSS through Resistance R, respectively, 3n of MOS transistors will be turned on by connecting the gate to a power terminal VDD through MOS transistor 4p, and MOS transistor 3p will become ** ON similarly by connecting the gate to a power terminal VSS through 4n of MOS transistors. Thereby, MOS transistors 3n and 3p connect between the input/output terminals of a CMOS inverter, and operate as a feedback resister by the on resistance. This example performs oscillation operation like the conventional thing, and generates an oscillation output signal from an output buffer 5.

[0011] Here, with static electricity etc., if the high voltage is impressed to the external terminal XT, an overvoltage will join a power-terminal VDD side through the gate of 3n of MOS transistors and the drain of MOS transistor 4p, and the source from an input terminal IN. At this time, it is mitigated by the on resistance of MOS transistor 4p, and the overvoltage impressed to the gate of 3n of MOS transistors can avoid gate destruction of 3n of MOS transistors. Moreover, the same is said of MOS transistor3p, and it is mitigated by the on resistance of 4n of MOS transistors, and the overvoltage by which gate impression of the MOS transistor 3p is carried out can avoid gate destruction.

[0012] If the transistor size of MOS transistors 4n and 4p is suitably set up as mentioned above, MOS transistors 4n and 4p can set an on resistance as a desired value. And when this example is integrated, compared with the resistance which these MOS transistors 4n and 4p become from the usual conductive layer, high resistance is obtained in a small occupancy area. That is, suitable resistance is obtained, without making the size of the resistance connected like the conventional thing between the gates of an MOS transistor and the power terminals which constitute a feedback resister increase, in order to avoid above-mentioned gate destruction, as a result the increase in a chip size can be suppressed.

[0013] Moreover, it is good also as preparing only either not only among two MOS transistors of MOS transistors 3n and 3p constituting a feedback resister like the one above-mentioned example but among MOS transistors 3n and 3p, and this constituting a feedback resister.

[0014] moreover, in the one above-mentioned example, as a piezoelectric transducer although a quartz resonator is used, restrict to this -- it is not **, for example, ceramic vibrators, such as a PZT system and PbTiO3 system, may be used

[0015]

[Effect of the Invention] According to this invention, it becomes possible to offer the integrated circuit for an oscillation and an oscillator circuit excellent in the endurance over static electricity, without making circuit area increase.

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1] The integrated circuit for an oscillation characterized by providing a CMOS inverter, having connected the feedback resister which consists of an MOS transistor between the input/output terminals of the above-mentioned CMOS inverter in the integrated circuit for an oscillation by which external is carried out in a piezoelectric transducer between the input/output terminals of the above-mentioned CMOS inverter, and holding the gate of the above-mentioned MOS transistor to specific potential through the 2nd MOS transistor.
[Claim 2] The oscillator circuit characterized by having connected the feedback resister which consists of an MOS transistor between the input/output terminals of the above-mentioned CMOS inverter in the oscillator circuit which comes to connect a piezoelectric transducer between the input/output terminals of the above-mentioned CMOS inverter, and holding the gate of the above-mentioned MOS transistor to specific potential through the 2nd MOS transistor while connecting load-carrying capacity to each of the input terminal of a CMOS inverter and the above-mentioned CMOS inverter, and an output terminal.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The electrical diagram showing the composition of one example of this invention.
[Drawing 2] The electrical diagram showing the composition of a Prior art.
[Description of Notations]
1 CMOS Inverter
2 Quartz Resonator
3 Feedback Resister
3n, 3p MOS transistor
4n, 4p MOS transistor (the 2nd MOS transistor)

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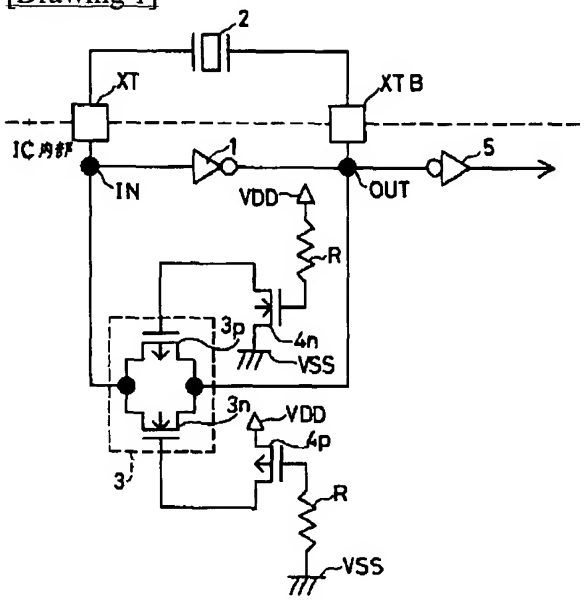
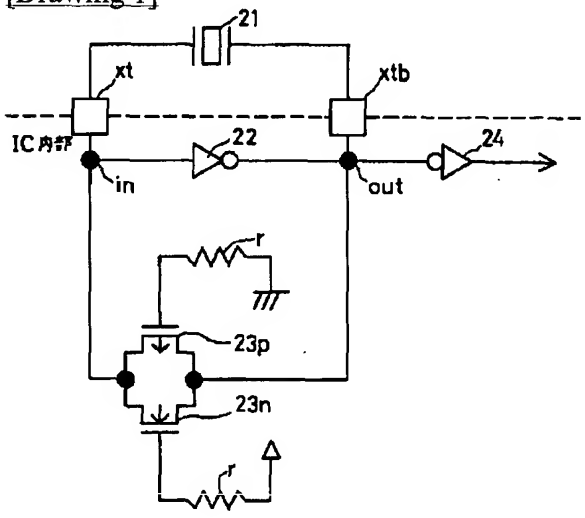
DRAWINGS

[Drawing 1]



[Drawing 1]



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